



Considerations for Use of Endwave Surface Mount Packages

1. Scope

This document describes highlights several points to be considered to achieve optimal outcomes when using microwave or millimeterwave QFN surface mount technology devices as mounted to printed circuit boards (PCBs). As a provider of over 600k subsystems which use millions of our own MMICs, our experts have drafted this document to share their insights which may be discussed in depth by calling (877) endwave.

2. Storage

Devices should be stored in a humidity controlled and static free area. All Endwave QFN and DFN surface mount devices are rated MSL3 or better, whether air cavity or plastic overmold technologies are used. MSL2 and MSL3 devices will be clearly identified as such on the device tray, rail or package reel. Additional marking will appear on the intermediate moisture barrier bag. The bag will contain a humidity indicating card and silica gel desiccant.

3. Solder process design considerations

All Endwave QFN and DFN devices are ROHS compliant. Palladium gold terminations ensure full compatibility with both ROHS and non ROHS smt processes.

Maintaining proper solder coverage, both beneath the center ground paddle and at the outer leads is critical. The effect of the solder coverage (or lack of coverage) will enhance or impact both thermal and RF performance, while consistent control of coverage leads to higher repeatability. To ensure proper control, the solder stencil opening should consider the specific solder volume required. For leadless flat devices such as QFN and DFN, there should be particular attention for the center ground paddle.

The required solder will be dependent on:

- Specific device lead geometry
- PCB solder mask
- Via features (tented filled etc.) and size.

The amount of solder dispensed for a solder stencil process depends largely on:

- Stencil manufacturing specification, where a laser cut and electro-polished stencil is preferred to reduce variability in the amount of solder dispensed.
- Stencil opening
- Stencil thickness
- Solder mesh size
- % of solder in the paste per volume
- Squeegee type as well as speed and pressure

Too much solder on the ground paddle and/or excessive voiding can cause the device to “float” on the ground paddle solder, potentially compromising both performance and reliability.

The two issues including excessive solder or excessive solder voiding under the device must be properly differentiated in order to troubleshoot a sub-optimal process, while either can cause the installed device to appear tilted on the PCB – and therefore may produce the same externally visible effect. For this reason, it should be noted that the root cause of a sub-optimal result cannot be differentiated from one another by visual inspection alone.

4. Troubleshooting the process

In this example, the multilayered PCB under the ground paddle contains an array of filled and copper capped vias, where a cross section of the PCB through 1 of the vias is shown in Figure 1, below.

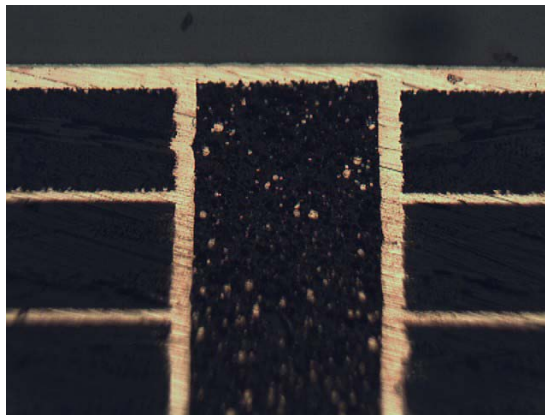


Figure 1: Filled and copper capped via.

On top of this array of vias there is a 24 lead QFN device mounted, where it can be seen that the device is lifted away from the pcb on one side – adversely affecting performance. The tilting effects the outer leads of the device most profoundly, where in this case a critical RF pad is affected. From a visual assessment only, it could be interpreted that the device has excessive solder dispensed at the ground paddle. As will be demonstrated, a further examination using an x-ray provides the insight required to solve the issue.

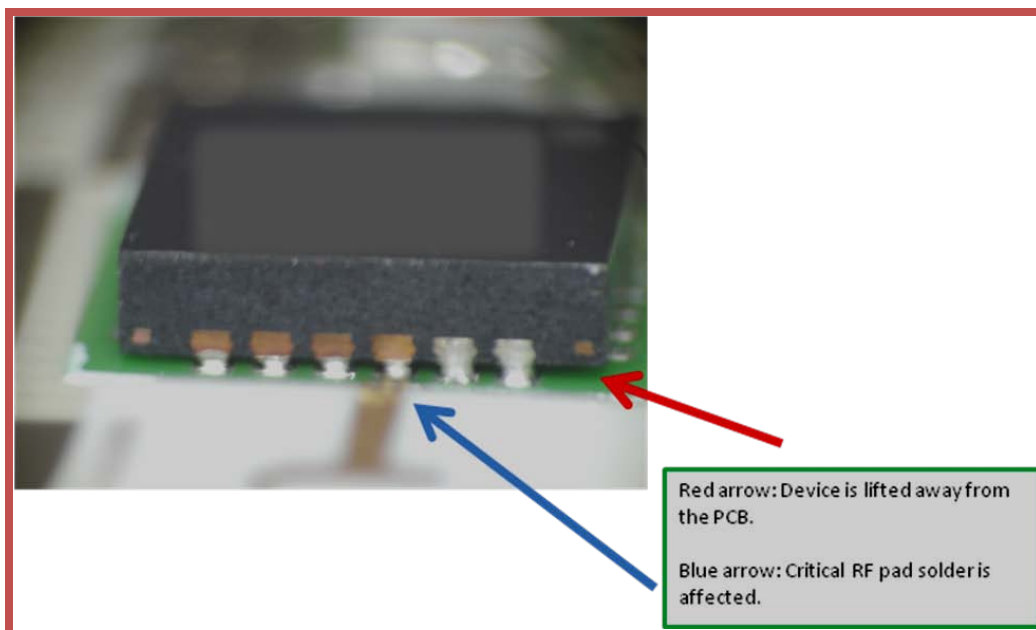


Figure 2: 4x4x24 device tilted on the PCB.

Examination of an x-ray reveals the likely cause of the tilting and resultant solder issues is due to excessive voiding, as depicted by the light gray areas between the uniformly spaced via holes. Attention to the solder reflow profile may be required to solve this issue.

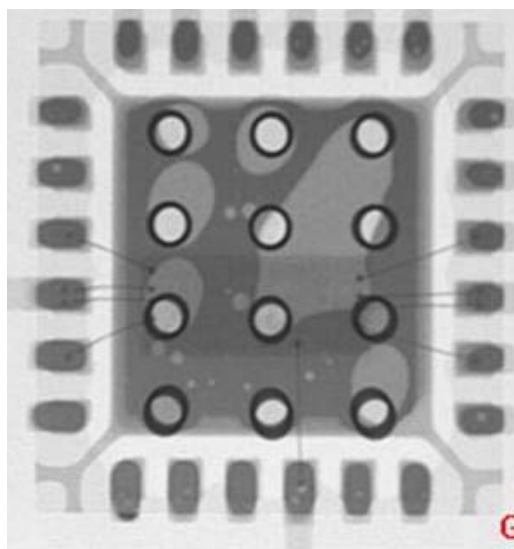


Figure 3: X-ray of the device.

Figure 4 demonstrates a close up of the upper right solder, where the red circled area is the device lead outline. In this case, the area of the device is raised from the PCB, where the blue circled area shows the solder does not fill the lead outline, but rather a small section of it – resulting in a suboptimal outcome.

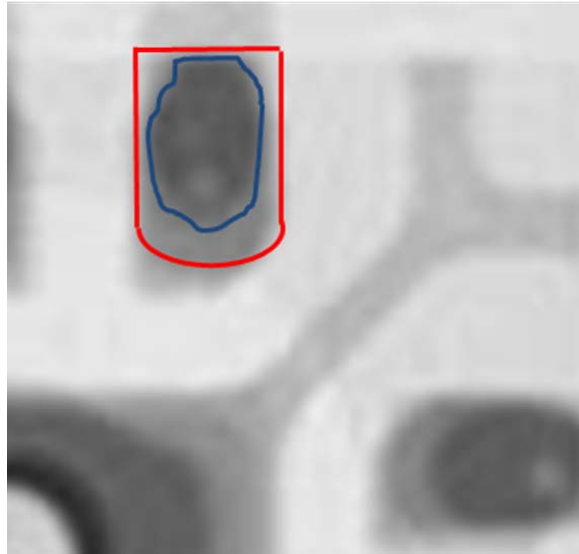


Figure 4: X-ray close-up of an improperly soldered device lead.

On the contrary, Figure 5 demonstrates a close-up of the lower left solder area, where the red circled area is again the device lead outline. This area of the device is down properly to the PCB, as the solder completely fills the lead outline.

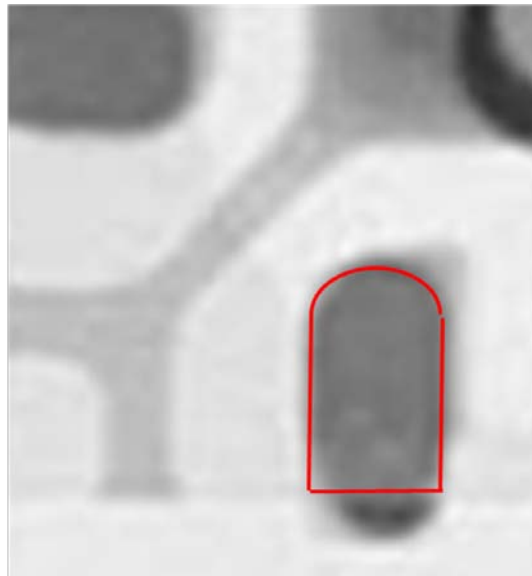


Figure 5: X-ray close-up of a properly soldered device lead.

A visual of a properly mounted 4x4x24 lead QFN is shown in Figure 6, and is provided to demonstrate the result of proper solder coverage of the outer leads, resulting in a flat spacing from the PCB, and good solder performance.

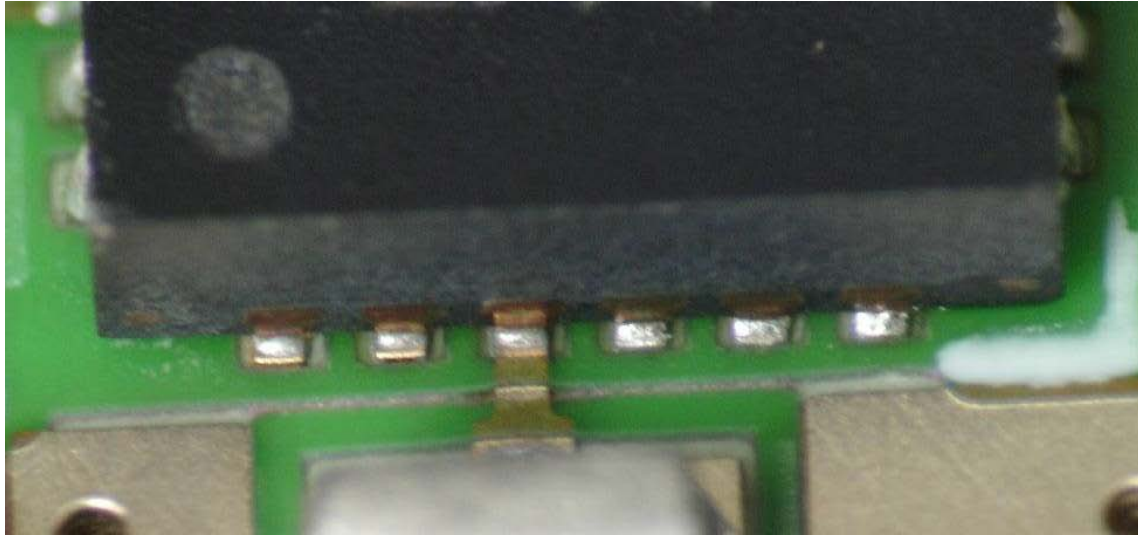


Figure 6: Proper mounting and solder coverage for a 4x4x24 device on a PCB.

The important note to take away from this discussion is that careful attention to both the solder profile and the solder stencil design for the specific pcb layout is critical. The solder profile must be correct before the solder dispense volume can be judged as optimized. Proper examination by x-ray is recommended.

5. Via construction types

Each of the via types shown will affect the required solder.

(a) Filled and copper capped via.

Pro: Most stable thermal performance and best control of the solder process.

Con: Higher PCB processing cost compared to normal thru via.

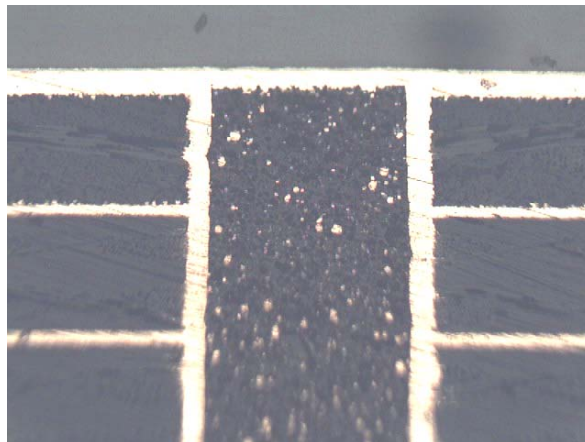


Figure 7: PCB cross section through a copper capped via

(b) Filled and un-capped via.

Pro: Stable thermal performance and good solder process control.

Con: Higher pcb processing cost compared to normal thru via.

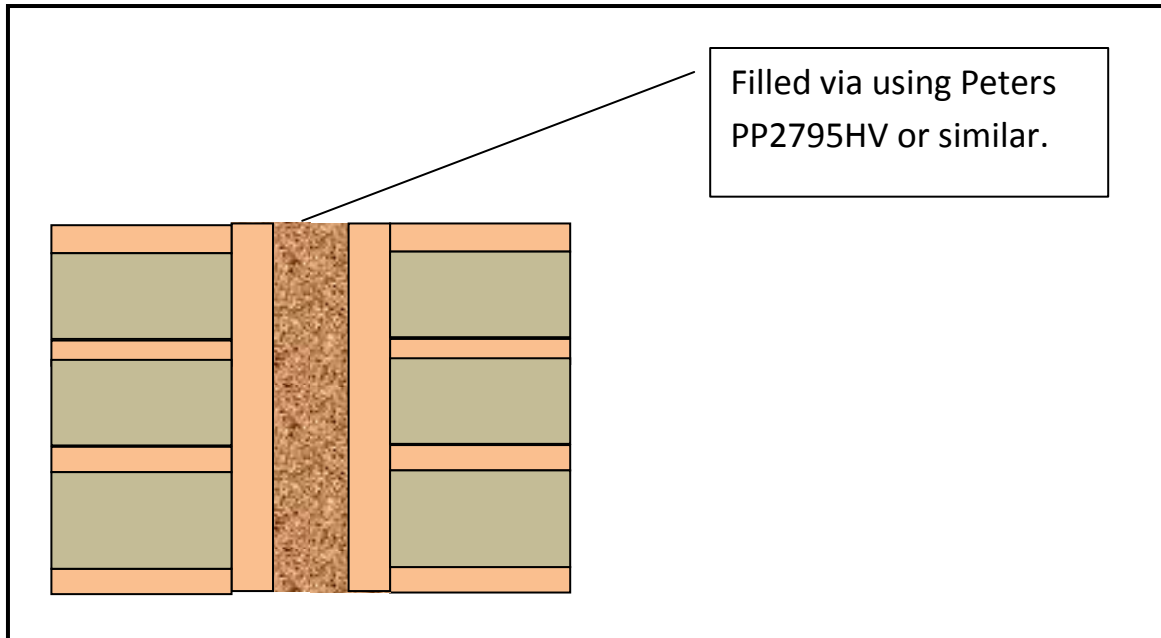


Figure 8: PCB cross section through a filled and un-capped via

(c) Dry film tented via.

Pro: Reduced PCB processing cost with good solder process control.

Con: Limited thermal performance.

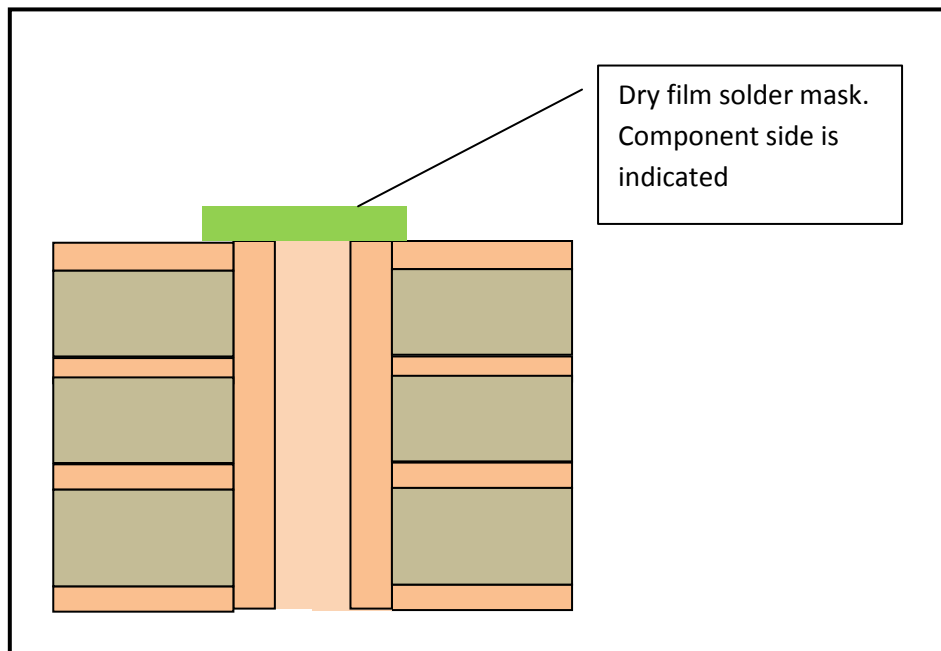


Figure 9: PCB cross section through a dry film tented via

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(d) Through via.

Pros: Least expensive pcb processing cost.

Con: May result in reduced solder process control.

Least stable thermal performance.

Both are due to solder wicking at the vias. The effect is more apparent for high aspect ratio vias.

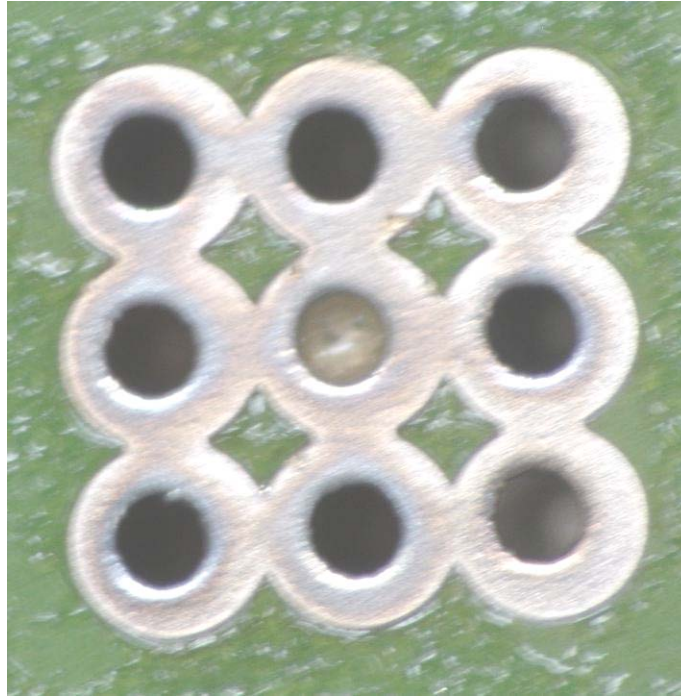


Figure 10: Top view of through via array

(e) Solder paste plugged via.

While several PCB fabrication houses may discuss this technology as a low cost option, the use of vias plugged with solder mask under any type of component is not recommended, as the stability of the solder mask versus temperature may cause a destructive force on the solder joint due to expansion of the solder mask during the cure phase. Solder mask may extrude from the via during re-flow causing the device to be raised from the PCB. The effect is more pronounced as the depth of the plugging is increased.

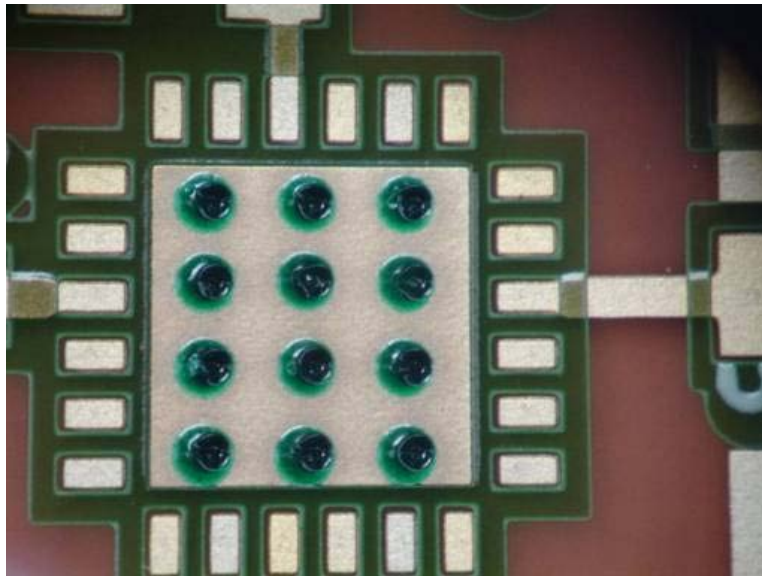


Figure 11: Top view of through via array filled with solder mask after cure